Printed Circuit Boards
Part I – Overview

Robert S. Balog Jr., PE
Overview – Part I

- Motivation
- Cost issues
- PCB Design Process
- Post Design Process
- PCB Manufacturing Overview
PCB Advantages

• Reliability of design
  – Tight circuit design
  – No loose wires to pop-out

• Repeatability of experiments
  – Physically rugged
  – Archival design
  – No “black magic” to recreate original results

• Control of geometric considerations
  – Stray inductances and capacitances

• Cost of development
  – Time spend wire-wrapping and debugging vs. PCB design

• Marketable engineering skill
PCB Disadvantages

• Learning Curve
  – Software
  – Layout skills
  – DFM – Design for Manufacturability

• Investment in time to create custom footprints.
  – Up-front investment in time
  – Mitigated by UIUC library of known good parts

• Fixed cost of PCB order
PCB Development Investment

Up-front vs. back-end costs

- PCB design: large initial investment
- Vector board: trouble shooting / debugging commitment
- Archival issues:
  - Cost recovery by communizing on parts in laboratory
  - Re-use known-good footprints
PCB Vendor Cost Drivers

- **Material**
  - $0.167 per sq in. on prototype order
  - $0.153 per sq in on 50k production order

- **Time**
  - Engineer time – CAM review
  - Machine time
  - Delivery / shipping
    - Pay for fast turn → use UPS RED
Delivery Schedule

How fast do you need it? I.e. a little bit of planning...

- Prototype Service:
  - Fast board turn options
  - Tooling costs included
  - Limitations on process capability (usually sufficient for our purposes)
  - 3 days → 1 day: 96% premium (5pcs. 5” x 6”)

### PROTOTYPE Price Matrix - unit price

<table>
<thead>
<tr>
<th>Qty</th>
<th>5-day</th>
<th>4-day</th>
<th>3-day</th>
<th>2-day Best Value!</th>
<th>1-day</th>
<th>same-day</th>
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<tbody>
<tr>
<td>5</td>
<td>N/A</td>
<td>N/A</td>
<td>$72.20</td>
<td>$87.20</td>
<td>$142.20</td>
<td>$182.20</td>
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<td>10</td>
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<td>N/A</td>
<td>$44.40</td>
<td>$51.90</td>
<td>$79.40</td>
<td>$99.40</td>
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</tbody>
</table>

- 3 for $33 ea. Special:
  - 5 day lead time
  - Limited process capability (1oz only)
  - Max. 85 sq. in. (8.5” x 10”)
  - 33 special → 3 day proto service: 118% premium (5 pcs)
Delivery Schedule

How fast do you need it? It’s a little bit of planning...

- Production Service:
  - Fast board turn options
  - Tooling costs extra
  - Lowest cost in quantity
  - Designed for higher volume, longer delivery schedules
  - Full production capability
  - 2 weeks → 3 days: 43% premium (50k pcs. 5” x 6”)

<table>
<thead>
<tr>
<th>Qty</th>
<th>4-week</th>
<th>2-week</th>
<th>1-week</th>
<th>4-day</th>
<th>3-day</th>
<th>2-day</th>
<th>1-day</th>
<th>same-day</th>
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<tr>
<td>5</td>
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<td>$48.43</td>
<td>$55.34</td>
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<td>$89.93</td>
<td>$134.90</td>
<td>$169.49</td>
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<td>$6.64</td>
<td>$7.58</td>
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<td>$23.23</td>
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<tr>
<td>50000</td>
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<td>$7.35</td>
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<td>$11.94</td>
<td>$17.91</td>
<td>$22.51</td>
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</tbody>
</table>

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Design Process

1. **Electrical Circuit Design**
   - Topologically correct, critical values (caps, inductors, power R)
   - Breadboard tested
   - Design review with PI, Jonathan Kimball

2. **Documentation**
   - Review ECE Power Design Archives specification file:
     SD00001-001 PCB File Management.doc

3. **Cadence Orcad Capture CIS v10.1 (PSD 15.1)**
   - Topological schematic
   - Logical flow not physical flow
   - DRC

4. **Cadence Orcad Layout Plus v10.1 (PSD 15.1)**
   - Signal / power flow
   - Component footprints
   - Padstacks
   - DRC
Post-Design Process

1. Don’t rush. Up to 3pm counts as day #1
2. DRC (Design Rule Check)
   Schematic
   Layout
3. FREE DFM at Advanced Circuits
   Only examples of errors, not each occurrence
   Fix errors and Re-run
4. Order
   Upload Data
   Coordinate with Jonathan Kimball to place order
5. Watch e-mail
   Within 1st day on-hold notice if problems
## Design Considerations

<table>
<thead>
<tr>
<th></th>
<th>Cost Driver</th>
<th>Design Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Material</td>
<td>Machine time</td>
</tr>
<tr>
<td>Panel Utilization</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Layer Count</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Copper Thickness</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td># hole sizes</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Minimum hole size</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal corners</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Trace Spacing</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Copper Weight

1 oz of copper will cover 1 sq. ft. when rolled out to a thickness of 0.0014” or 1.4 mil

Copper Weight/Thickness Table

<table>
<thead>
<tr>
<th>Weight</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/2 oz.</td>
<td>0.0007</td>
</tr>
<tr>
<td>1 oz.</td>
<td>0.0012” - 0.0014”</td>
</tr>
<tr>
<td>2 oz.</td>
<td>0.0028</td>
</tr>
</tbody>
</table>
Printed Circuit Boards
Part II – Manufacturing

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Overview – Part II

- Structure
- Core Laminate
- Drilling
- Photo imaging process
- Photo tools
- Solder Mask
- Finishes
- Legend
- Routing
Printed Circuit Board

Rigid Laminate material (FR4, typ.) consisting of a glass epoxy substrate clad with copper on two sides for double side (0.062” typ.)

Typically in sheets at ½ oz. and 1 oz. Per square foot in weight (0.0007 and 0.0014 inches nominal thickness respectively).
Prepreg

Multilayer “glue”
Woven Fiberglass cloth pre-impregnated with partially cured epoxy resin
Also known as B-stage
The Resin is activated and “melts” during the lamination process from pressure and heat.
It flows across oxide coating on the core to create bond.
Primary Drilling

Holes are drilled through a stack of panels (usually 2 to 3 high)

Drilled hole sizes are typically 5 mils larger than finished plated through hole sizes
Dry Film Photo Resist

Light sensitive film is applied, using heat and pressure, to the copper surfaces of the laminated panel. Film also covers, or tents, all drilled holes.
Photo Tools (Artwork)

The gerber data for the panel is used to plot film that depicts the circuits and traces of the board. The photo tools or artwork includes solder mask and nomenclature or legend too.

File Names

*.TOP = Top Copper
*.BOT = Bottom Copper
*.SMT = Solder Mask Top
*.SMB = Solder Mast Bottom
*.SST = Silk Screen (legend) TOP
Expose

Panels are exposed to a high intensity light source coming through the film. Clear areas allow light to pass through and polymerize (harden) the film resist thus creating a latent image of the circuit pattern – just like a photograph.
Develop

The exposed core is passed through a chemical solution or developer that removes the resist from areas that were not hardened (polymerized) by the light.
Etch

Copper is chemically removed from the core in all areas not covered by film resist.
This creates a discrete copper pattern that matches the film pattern.
The core laminate surface now shows through in areas where copper was etched away.

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Strip Resist

The developed dry-film resist is now chemically removed from the panel. The copper remains on the panel only in the patterns described by artwork.
Copper Pattern Plate

Also called electroplating, additional copper is electrically plated onto the exposed electroless copper surfaces.

The plated Copper thickness is approximately 1 mil, depending on the required final finish for the panel.
Solder Mask

SMOBC (Solder Mask Over Bare Copper)
LPI (Liquid Photo-Imageable) 8mil resolution

A photo-sensitive liquid mask is applied to the front and back surface of the panel. It is then dried to the touch (referred to as tack-dry), but not cured. Artwork is applied and exposed and the panel is developed leaving mask in pattern described by artwork.
Finish Plating:

- Hot Air Solder Level (HAL or HASL)
- Hard Gold – electro plated gold
- Electro less Nickel Emersion Gold
- White Tin
- Organic Solderable Preservative (OSP)
Hot Air Solder Leveling (HASL)

Panels are processed through a bath of molten solder, covering all exposed metal surfaces. High pressure hot air, directed at both sides of the panel simultaneously, removes excess solder from the holes and surfaces.
Legend (Silk Screen)

Ink is silkscreened onto one or both sides of the panel. This is purely an annotation detail typically consisting of component orientation outlines, reference designators, etc.
Route, Score, and Bevel

Score lines help in de-panelization.
Routing cuts the boards to size.
Electrical Test

Boards are tested for electrical integrity (opens and shorts in circuitry) Data can be directly loaded onto various types of test machines or used to create fixtures and net list programs.

Flying Probe test machine.
Printed Circuit Board
Part III – Design Issues

Robert S. Balog Jr., PE
Overview – Part III

• Design aspects:
  – Mechanical Considerations
  – Routing Strategies
  – Why Auto-Routers are bad
  – Current Capability and Voltage Spacing

• DFM:
  – Trace / Space Aspect Ratio
  – Manufacturing dictates clearances
  – Pad Stack
  – Pad Exits

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Mechanical Issues

- 1st Quadrant Design (Pos x,y)
- Board dimensions:
  - Will this fit an enclosure?
  - 16”x20” Max panel size
- Mounting method:
  - Rubber feet
  - Standoffs / spacers
  - Clearance hole size for screws
- Off-Board Connectors:
  - Clearance requirements
Routing Methodology

- Place Components
- Route power and ground
- Route high speed busses
- Route sensitive analog nets
- No vias under components
Auto-Routing?

- In general it is a poor algorithm for power electronics
- Based on grids
  - Top layer in one direction
  - Bottom layer in other
  - Vias as interconnects
- At best it will connect the nodes
- At worst you will have a circuit with poor performance due to inductive and capacitive coupling
- If you feel compelled, do power and ground and high di/dt by hand first.
Copper Weight

1 oz of copper will cover 1 sq. ft. when rolled out to a thickness of 0.0014” or 1.4 mil

<table>
<thead>
<tr>
<th>Cu Weight</th>
<th>Min Cu</th>
<th>Min finished thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 oz</td>
<td>1.22 mil</td>
<td>2.08 Mil</td>
</tr>
<tr>
<td>2 oz</td>
<td>2.43 mil</td>
<td>3.30 mil</td>
</tr>
<tr>
<td>3 oz</td>
<td>3.65 mil</td>
<td>4.51 mil</td>
</tr>
<tr>
<td>4 oz</td>
<td>4.86 mil</td>
<td>5.69 mil</td>
</tr>
</tbody>
</table>

IPC-2221A “Generic Standards on Printed Circuit Board Design”
Current Carrying Capability*

\[ I = k \cdot \Delta T^{0.44} \cdot A^{0.725} \]

\[ \Delta T = T_{\text{Max}} - T_{\text{Ambient}} \]

\[ k = \begin{cases} 
0.048 \text{ outer layers} \\
0.024 \text{ inner layers} 
\end{cases} \]

\[ A = \text{Trace cross-sectional area} \]

*IPC-2221A “Generic Standards on Printed Circuit Board Design”
Current and Trace Thickness for a Temperature Rise of 20°C

- Trace Width [mil]
- Max Current [A]

4 oz
3 oz
2 oz
1 oz
Trace / Space / Weight

Large aspect ratio must take into account etch-back and plating factor.

Conductor width, thickness and spacing reduction of 30% allowed as per Advanced Circuits Spec.
Electrical Isolation

- **Creepage**: Shortest path between two conductive parts measured along the surface of the insulation.
  - Humidity in the atmosphere.
  - Presence of contamination.
  - Corrosive chemicals.

- **Clearance**: Shortest distance between two conductive parts measured through air.
  - Relative humidity
  - Temperature,
  - Pollution in the environment.
Electrical Isolation

- **Working Voltage:** Highest voltage insulation is subjected to when equipment is operating at its rated voltage and under normal conditions.
  - Peak value is used to determine the clearance
  - RMS value is used to calculate creepage.
Electrical Clearance

- IPC 2221A: AC and pulsed voltages > 200V must consider dielectric and capacitive effects of substrate in addition to spacing.

<table>
<thead>
<tr>
<th>Withstand Voltage</th>
<th>Min. Spacing (B2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-30</td>
<td>3.9 mil</td>
</tr>
<tr>
<td>31-150</td>
<td>24.0 mil</td>
</tr>
<tr>
<td>151-300</td>
<td>49.2 mil</td>
</tr>
<tr>
<td>301-500</td>
<td>98.4 mil</td>
</tr>
</tbody>
</table>
Thermal Issues

- Thermal generators:
  - Linear Regulators
  - Transistors
  - Transformers
  - Power Resistors

- Thermal susceptibility:
  - Analog IC’s
  - MOV, Transorbes, Zener Diodes
  - Electrolytic Capacitors
Pad Design

\[ D_{\text{min pad}} = D_{\text{finished hole max}} + 2 \cdot T_{\text{min annular ring}} + Tol_{\text{manf.}} \]
Drilled Hole

Plated Hole size tolerance of +/- 0.005”
Board Dimensional tolerance of +/- 0.010”
Plating thickness in the hole wall of 0.0008” minimum allowed

Ø Non-plated Drill
Copper Annular Ring

Best Practice 12 mil minimum annular Ring - Layout default is 10 mil. Large thru-hole parts need larger pads.
Solder Mask Relief

Solder mask mis-registration covering 180 degrees of through hole pad leaving a 0.002” annular ring allowed
Tolerance Allowance

Drill Registration Tolerance

Solder Mask Registration

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Clearance

Pad - Trace

Trace - Trace

Pad - Pad

- \( \varnothing 0.034 \)
- \( \varnothing 0.050 \)
- \( \varnothing 0.060 \)
- 0.010
- 0.010
- 0.010

- 0.012
- 0.070

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Pad exits: round pads
Pad exits: square pads
Silk Screen (Legend)

- 8 mil minimum line width at Advanced Circuits
- White is standard, others available
- Preferred Character:
  - 10 mil line width
  - 75 mil character height
  - 100 character
- Consistent orientation
- Preferred top to bottom, left to right part numbers
Gerber Data – 2 layer PCB

- Extended Gerber 3.4 Format with CR after each block and *
  as end of block character
- Create a PBxxxx.zip file
  PBxxxx.TOP    Top copper layer
  PBxxxx.BOT    Bottom copper layer
  PBxxxx.SMT    Soldermask Top
  PBxxxx.SMB    Soldermask Bottom
  PBxxxx.SST    Silk Screen TOP
  PBxxxx.DRD    Drill Drawing + board dimensions
  PBxxxx.tap    Excellon Drill File
  PBxxxx.lis    Aperture List
  PBxxxx.txt    This readme file
  total files: 9
Case Study

- Datum not at lower left corner
- No Layer Identification
- Traces not on orthogonal grid
- Vias under components, esp. resistors
  - Not tented ➞ electrically exposed
- Top side traces under resistors
- Legend width too small
- Legend orientation inconsistent
- Parts not grouped logically ex. R25 too far from ic
Select References

- [http://www.energy.ece.uiuc.edu/balog](http://www.energy.ece.uiuc.edu/balog)
- **IPC – 2221A**¹ “Generic Standard on PCB Design”
- **UL 8402**² “Insulation Coordination Including Clearance and Creepage Distances for Electrical Equipment”
- **ANSI/ISA S82.01**² “Safety Standard for Electrical and Electronic Test, Measuring, Controlling, and Related Equipment – General Requirements”
- **UL 746E** “Standard Polymeric Material used in Printed Wiring Boards”

¹CEME Holding, ²UIUC Grainger Holding